REMARKS

Claims 1, 2, 8, 9, 16, 20 and 21 through 34 are pending. In an office action dated September 12, 2002, claims 1 through 20 were rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,732,153 granted to Ohsawa (hereinafter "*Ohsawa*"). These rejections are respectfully traversed.

Ohsawa fails to provide a prima facie basis for the rejection of claims 1, 8, 9, 16, 20 and 21 through 34 under 35 U.S.C. 102(b), because it fails to disclose each of the elements of the claimed inventions. In regards to claim 8, *Ohsawa* fails to disclose that "at least one of the varying characteristics is a pixel characteristic determined using at least one additional pixel characteristic from at least ***one additional pixel.***" (Emphasis added). *Ohsawa* operates using rows of pixels. "As described above, when the outputs B.sub.1 and B.sub.2 covering ***five lines*** are located in the corresponding line-buffer groups 175a and 175b, a white succession detecting circuit 176 and a black succession detecting circuit 177 respectively determine whether the black or white edges of the subject picture element are successive." *Ohsawa*, col. 9, lines 55-60 (emphasis added). In regards to claim 9, *Ohsawa* fails to disclose that "at least one of the varying characteristics is ***a*** pixel intensity." (Emphasis added). In regards to claim 20, *Ohsawa* fails to disclose "the at least one of the varying characteristics is a pixel characteristic determined using at least one additional pixel characteristic from ***at least one*** additional pixel." (Emphasis added). As described above, *Ohsawa* operates using rows of pixels and not single pixels. In one exemplary embodiment, the present invention can detect an edge by using one additional pixel characteristic from one additional pixel, such as by moving from an analysis of pixel "E" in Figures 6 or 7 to an analysis of pixel "B." In this exemplary embodiment, the data values for pixels "A," "B," "C," and "D" would remain unchanged, and an edge occurring between pixels "B" and "E" could be detected by using one additional pixel characteristic from one additional pixel, by varying a single pixel intensity characteristic, or in other suitable manners. Unlike the present invention, *Ohsawa* requires reading additional rows of pixels, and therefore fails to provide a prima facie basis for the rejection of claims 1, 8, 9, 16, and 20.

CONCLUSION

In view of the foregoing remarks and for various other reasons readily apparent, Applicants submit that all of the claims now present are allowable, and withdrawal of the rejection and a Notice of Allowance are courteously solicited.

If any impediment to the allowance of the claims remains after consideration of this amendment, and such impediment could be alleviated during a telephone interview, the Examiner is invited to telephone the undersigned at (214) 969-4669 so that such issues may be resolved as expeditiously as possible.

No additional fee is believed to be due. If any applicable fee or refund has been overlooked, the Commissioner is hereby authorized to charge any fee or credit any refund to the deposit account of Akin, Gump, Strauss, Hauer & Feld, L.L.P., No. 01-0657.

Respectfully submitted,

Date: 12/12/02

Christopher J. Rourk
Registration No. 39,348
Attorney for Applicant

Akin, Gump, Strauss, Hauer & Feld, L.L.P.
P.O. Box 688
Dallas, TX 75313-0688
(214) 969-2800

VERSION SHOWING CHANGES MADE TO CLAIMS

2. **(AMENDED)** The image processing **system** of claim 1, further comprising a white edge detector **applying a dynamic white edge threshold**.

Claims 3 through 7 are hereby cancelled without prejudice or disclaimer.

Claims 10 through 15 are hereby cancelled without prejudice or disclaimer.

Claims 17 through 19 are hereby cancelled without prejudice or disclaimer.

21. **(NEW)** The image processing system of claim 1, further comprising a white edge detector comparing two or more pixels to a single test pixel.

22. **(NEW)** The image processing system of claim 1, further comprising a white edge detector comparing a single test pixel to a first adjacent pixel to generate a first difference, comparing the test pixel to a second adjacent pixel to generate a second difference, comparing the test pixel to a third adjacent pixel to generate a third difference, and comparing the test pixel to a fourth adjacent pixel to generate a fourth difference, and generating a white edge detection when any of the first difference or the second difference and the third difference or the fourth difference are greater than a threshold.

23. **(NEW)** The image processing system of claim 22 wherein the threshold is a dynamic threshold.

24. **(NEW)** The image processing system of claim 22 wherein the first adjacent pixel and the second adjacent pixel are not adjacent to each other.

25. **(NEW)** The image processing system of claim 1, further comprising a white edge

detector comparing a single test pixel to a first adjacent pixel to generate a first difference and comparing the test pixel to a second adjacent pixel to generate a second difference, and generating a white edge detection when the first difference and the second difference are each greater than a threshold.

26. **(NEW)** The image processing system of claim 1, further comprising a white edge detector comparing a single test pixel to one or more first adjacent pixels to generate a first difference and comparing the test pixel to one or more second adjacent pixels to generate a second difference, and generating a white edge detection when the first difference and the second difference are each greater than a threshold.

27. **(NEW)** An edge detection circuit comprising:

a first test pixel comparator comparing a test pixel to one or more first adjacent pixels, generating a first difference, and determining whether the first difference is greater than a first threshold;

a second test pixel comparator comparing the test pixel to one or more second adjacent pixels, generating a second difference, and determining whether the second difference is greater than a second threshold; and

an edge detector receiving the determination from the first test pixel comparator and the second test pixel comparator and generating an edge detection.

28. **(NEW)** The edge detection circuit of claim 27 wherein the first threshold and the second threshold are the same.

29. **(NEW)** The edge detection circuit of claim 27 wherein the first threshold and the second threshold are dynamic.

30. **(NEW)** The edge detection circuit of claim 27 wherein the first test pixel comparator further comprises:

a first sub-comparator comparing the test pixel to one of the first adjacent pixels to generate a first sub-difference and determining whether the first sub-difference is greater than a first sub-threshold;

a second sub-comparator comparing the test pixel to another of the first adjacent pixels to generate a second sub-difference and determining whether the second sub-difference is greater than a second sub-threshold; and

outputting an indication that the first difference is greater than the first threshold if either the first sub-difference is greater than the first sub-threshold or the second sub-difference is greater than the second sub-threshold.

31. **(NEW)** The edge detection circuit of claim 30 wherein the second test pixel comparator further comprises:

a third sub-comparator comparing the test pixel to one of the second adjacent pixels to generate a third sub-difference and determining whether the third sub-difference is greater than a third sub-threshold;

a fourth sub-comparator comparing the test pixel to another of the second adjacent pixels to generate a fourth sub-difference and determining whether the fourth sub-difference is greater than a fourth sub-threshold; and

outputting an indication that the second difference is greater than the second threshold if either the third sub-difference is greater than the third sub-threshold or the fourth sub-difference is greater than the fourth sub-threshold.

32. **(NEW)** The edge detection circuit of claim 31 wherein the first sub-threshold, the second sub-threshold, the third sub-threshold, and the fourth sub-threshold are the same.

33. **(NEW)** The edge detection circuit of claim 31 wherein the first sub-threshold, the second sub-threshold, the third sub-threshold, and the fourth sub-threshold are dynamic.

34. **(NEW)** The edge detection circuit of claim 31 wherein the one of the first adjacent pixels is not adjacent to the other of the first adjacent pixels, and the one of the second adjacent pixels is not adjacent to the other of the second adjacent pixels.